MINISTRY OF EDUCATION AND SCIENCE OF RUSSIAN FEDERATION

MOSCOW POWER ENGINEERING INSTITUTE (TECHNICAL UNIVERSITY)

Vishnyakov S., Vishnyakova Y.

Modeling of electronic circuits Laboratory works 1-4

Workbook on "Electronics" for English-speaking students studying "Informatics and Computer Engineering" (230100) at the Moscow Power Engineering Institute

Edited by M. Tchobanou

Moscow MPEI publishing house 2011

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Утверждено учебным управлением МЭИ
в качестве методического пособия по курсу «Электроника» для студентов, обучающихся по направлению 230100 «Информатика и вычислительная техника» на английском языке
Моделирование электронных цепей. Лабораторные работы 1-4. Вишняков С.В., Вишнякова Ю.Н., под ред. Чобану М.К. -М.: .издательский дом МЭИ. 2011. -16 с.

Modeling of electronic circuits. Laboratory works 1-4.
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Book consists of following laboratory works:
1. Elementary circuits with diodes;
2. Elementary circuits with bipolar transistors;
3. Elementary circuits with field-effect transistors;
4. Logic gates and their applications
which relates to basic parts of the Electronics course for English-speaking foreign students of Automation and Computer Science Department of Moscow Power Engineering Institute. Each laboratory work description includes preliminary and comprehension check questions. All works are based on the electronic circuit simulation with Design Center software.

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Laboratory work 1

Elementary circuits with diodes

Content: p-n junction models, numerical modeling of nonlinear circuits, semiconductor diode characteristics, elementary circuits with semiconductor diodes – rectifiers.

Before work

a. Read the lectures on semiconductor physics, p-n junctions, semiconductor diodes and rectifiers.
b. Draw an approximate volt-amps curve for semiconductor diode, for Zener diode.
c. Draw the schemes of half-wave and full-wave (bridge) circuits. Draw approximate voltage figures for their outputs.
d. Draw the scheme of voltage limiter (with two Zener diodes). Draw an approximate voltage figure for its output.

Laboratory assignments

Virtual experiment 1

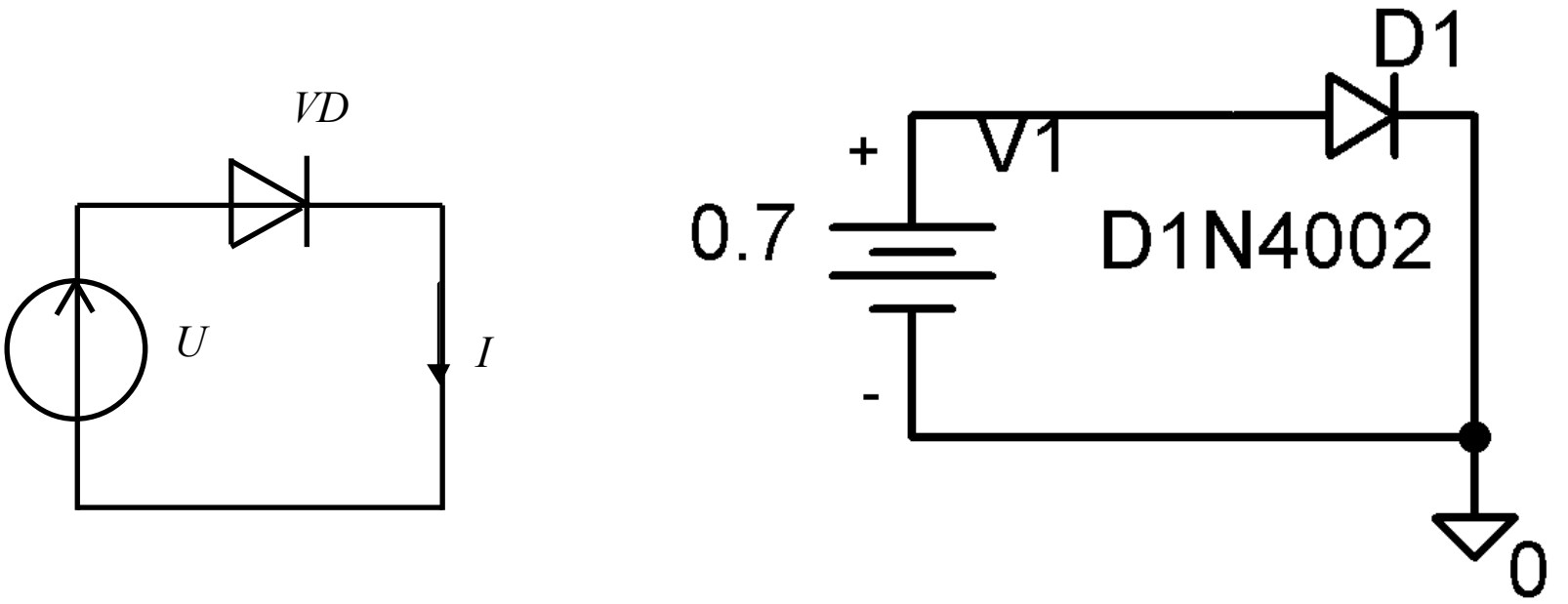

Figure 1. Scheme for virtual experiment 1

VE 1.1. In Design Center program (Schematic unit) draw a scheme of virtual experiment as shown on fig. 1.
Use following parts: "**VDC**" as a voltage source (battery); "**D1N4002**" as a model of power silicon diode 1N4002; "**agnd**" as a ground (zero potential) sign.

VE 1.2. Change voltage source attribute value (voltage *U*), simulate circuit and measure current (*I*) in the circuit to complete following table:

U, V	-1	-0.5	0	0.25	0.5	0.6	0.7	0.8	0.9	1.0
I, A			0							

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VE 1.3. Draw a volt-amps characteristic of silicon diode 1N4002.

VE 1.4. Change the reference temperature to 50°C and repeat steps **VE 1.2** and **VE 1.3.** Change the reference temperature back. To do it enter **Analysis-Setup** menu, push "**Temperature**" button and enter proper temperature (default value is 27°C).

Virtual experiment 2

VE 2.1. Replace model of diode 1N4002 by the part "D1N750" (model of silicon Zener diode (stabilitron) 1N750).

VE 2.2. Change voltage source attribute value (voltage *U*), simulate circuit and measure current (*I*) in the circuit to complete following table:

U, V	-6	-5	-3	-1	-0.5	0	0.25	0.5	0.6	0.7	0.8	0.9	1.0
I, A						0							

VE 2.3. Draw a volt-amps figure of silicon Zener diode 1N750.

Virtual experiment 3

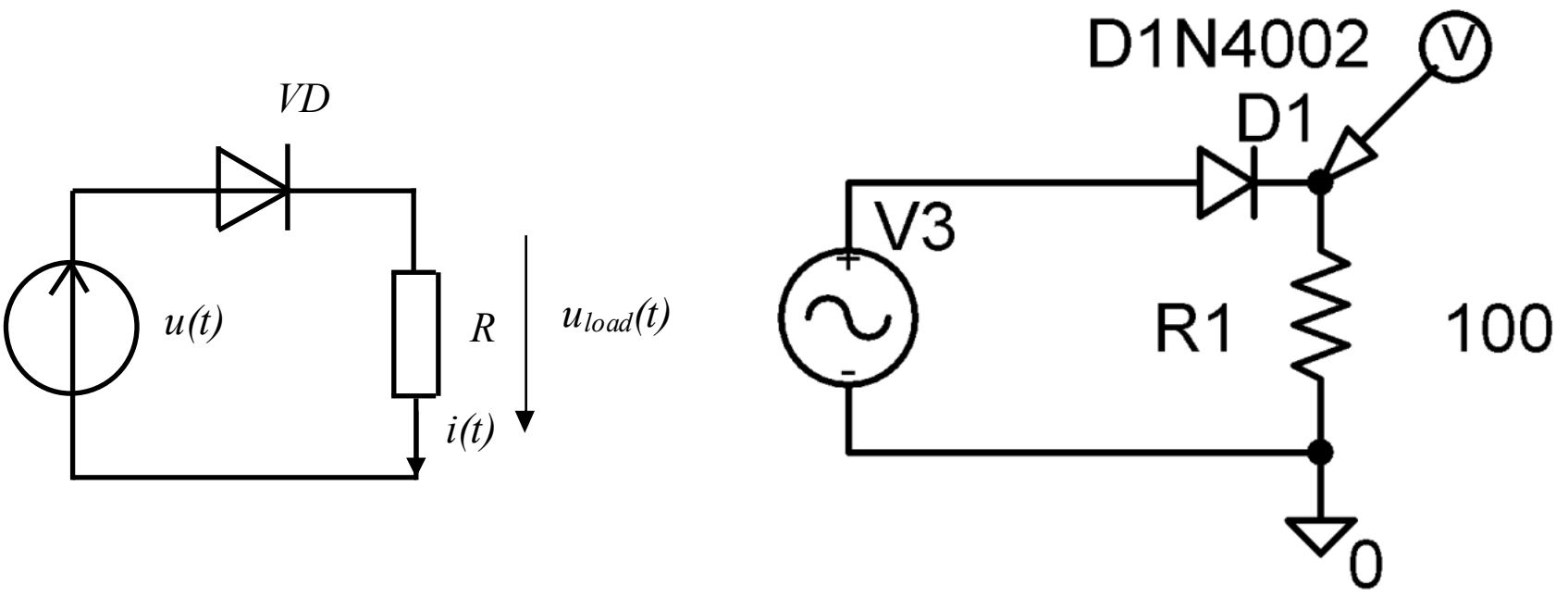

Figure 2. Scheme for virtual experiment 3

VE 3.1. Draw a scheme for half-wave circuit as shown on fig. 2.

Use following parts: "**VSIN**" as an alternating current (AC) generator; "**D1N4002**" as a model of power silicon diode 1N4002; "**r**" as a load resistor; "**agnd**" as a ground (zero potential) sign; **voltage and current probes** as shown on fig 2.

Set the value of the load resistor to 100 Ohm, frequency of voltage source to 50 Hz, amplitude of voltage source to 10V, starting phase angle to 0.

Check **Transient** box in **Analysis-Setup** menu, enter the **Transient** dialogue box and set following parameters: **Print Step** = **Step ceiling** = 0.0001; **Final time** = 0.1.

VE 3.2. Simulate circuit and print (or copy-paste) the voltage curves. Explain the results.

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VE 3.3. Add a parallel capacitor to refine output voltage. Capacity is to be calculated for 10% ripple rate.
Use the part "**c**" for capacitor.
Ripple rate is approximately estimated as $\frac{200\%}{CRf}$.

VE 3.4. Simulate circuit and print (or copy-paste) the voltage curves. Explain results.

Virtual experiment 4

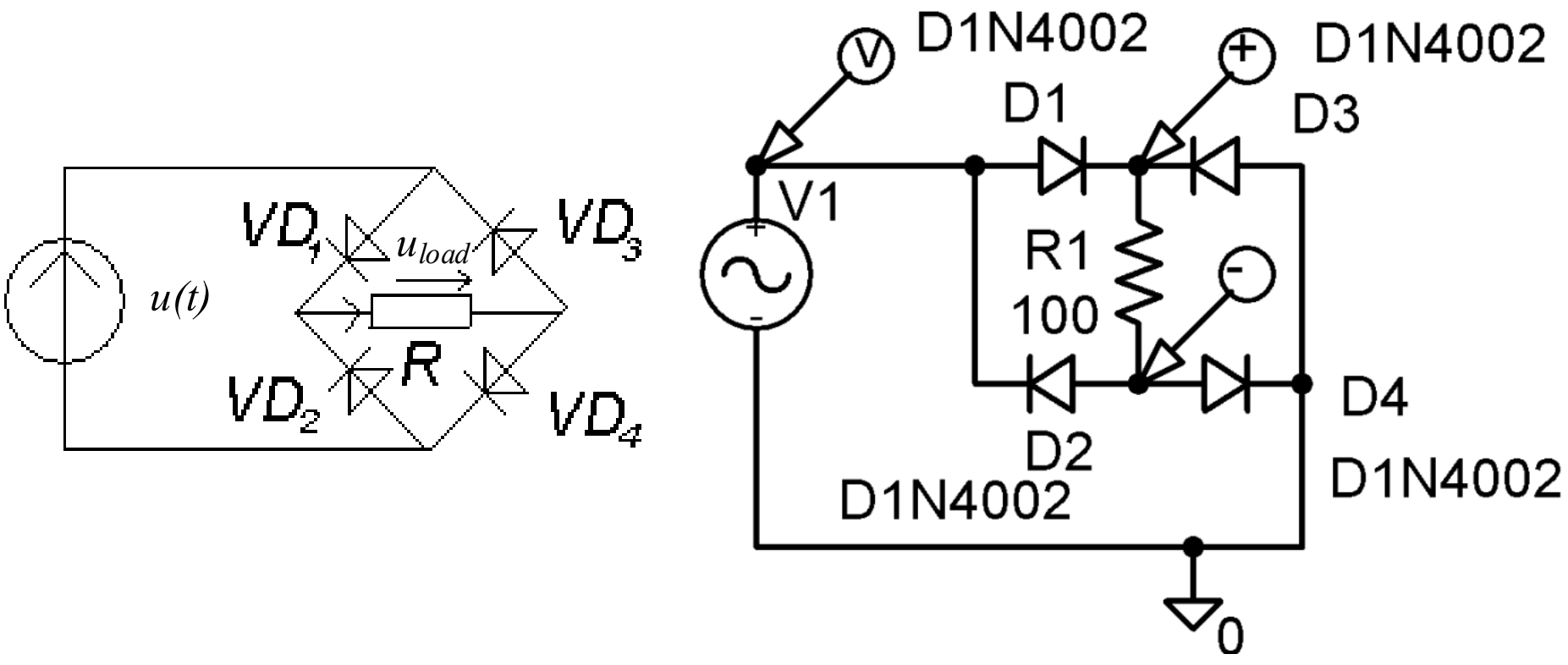

Figure 3. Scheme for virtual experiment 4

VE 4.1. Draw a scheme for full-wave (bridge) circuit as shown on fig. 3.
Use following parts: "**VSIN**" as an AC generator; "**D1N4002**" (four parts) as a model of power silicon diode 1N4002; "**r**" as a load resistor; "**agnd**" as a ground (zero potential) sign; **voltage** and **voltage difference** probes as show on fig 3.
Set the resistance of load resistor to 100 Ohm, frequency of voltage source to 50 Hz, amplitude of voltage source to 10V, starting phase angle to 0.
Check **Transient** box in **Analysis-Setup** menu, enter the **Transient** dialogue box and set following parameters: **Print Step** = **Step ceiling** = 0.001; **Final time** = 0.1.

VE 4.2. Simulate circuit and print (or copy-paste) the voltage curves. Explain the results.

VE 4.3. Add a parallel capacitor to refine output voltage. Capacity is to be calculated for 10% pulse rate.
Use the part "**c**" for capacitor.
Pulse rate is approximately estimated as $\frac{100\%}{CRf}$.

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VE 3.4. Simulate circuit and print (or copy-paste) the voltage curves. Explain the results.

After work

Answer following questions:

a. What is the differential resistance (conductivity) and how is it derived from volt-amps characteristic?
b. How does differential resistance of semiconductor diode depend on applied voltage?
c. How does differential resistance of semiconductor diode depend on temperature?
d. What is the difference between breakdowns in diode and Zener diode?
e. Draw current curves for each branch of the bridge circuit (without capacitor).
f. Draw current curves for each branch of the bridge circuit (with capacitor).

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Laboratory work 2

Elementary circuits with bipolar transistors

Content: bipolar transistors, their characteristics, NPN transistor with common (grounded) emitter in normal and saturated modes, differential amplifier on NPN transistors.

Before work

a. Read the lectures on semiconductor physics, p-n junctions, bipolar transistors, NPN transistor modes, linear amplifier on NPN transistor with common emitter, NPN transistor in switcher mode (electronic switcher) and differential amplifier on NPN transistor pair.
b. Draw approximate volt-amps curves of NPN transistor (base-emitter voltage vs. base current and collector-emitter voltage vs. base current).
c. Draw a scheme of linear amplifier on NPN transistor with common emitter. Write down formulas and equations for this circuit.
d. Draw a scheme of differential amplifier (current mirror scheme) on pair of bipolar NPN transistors. Draw a sketch of input-output figure.

Laboratory assignments

Virtual experiment 1

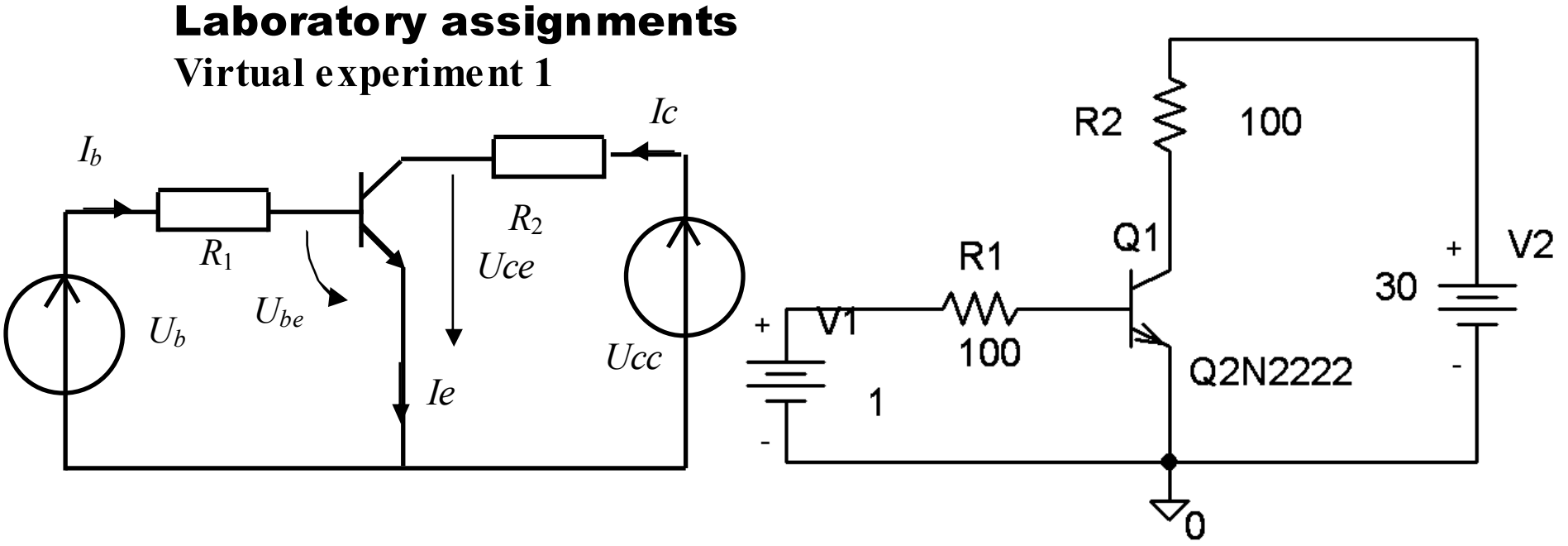

Figure 1. Scheme for virtual experiment 1

VE 1.1. In Design Center program (Schematic unit) draw a NPN transistor with common emitter scheme as shown on fig. 1.
Use following parts: "**Q2N2222**" as a model of silicon NPN transistor 2N2222; "**r**" (two parts) as resistors; "**VDC**" (two parts) as models of direct current (DC) sources; "**agnd**" as a ground (zero potential) sign.
Set both resistances to 100 Ohm.
Set power supply source (*Ucc*) to 30 V.

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VE 1.2. Change base voltage source value (voltage *Ub*), simulate circuit and measure collector-emitter voltage (*Uce*), base-emitter voltage (*Ube*), base and emitter currents (*Ib* and *Ie*) in the circuit to complete following table:

Ub, V	-1	0	0.6	0.7	0.75	0.8	0.9	1.0	1.1	1.5
Uce, V										
Ube, V										
Ib, A										
Ie, A										

VE 1.3. Draw volt-amps characteristic of NPN transistor: base current vs. base-emitter voltage.

VE 1.4. Change base voltage source value (voltage *Ub*) and collector voltage source (*Ucc*), simulate circuit and measure collector-emitter voltage (*Uce*), base-emitter voltage (*Ube*), base and emitter currents (*Ib* and *Ic*) in the circuit to complete following table:

Ub, V	0.8					1.0				
Ucc, V	30	25	20	15	10	30	25	20	15	10
Uce, V										
Ube, V										
Ib, A										
Ic, A										

VE 1.5. Draw volt-amps characteristic of NPN transistor: collector current vs. collector-emitter voltage (two curves for different *Ub*).

Virtual experiment 2.

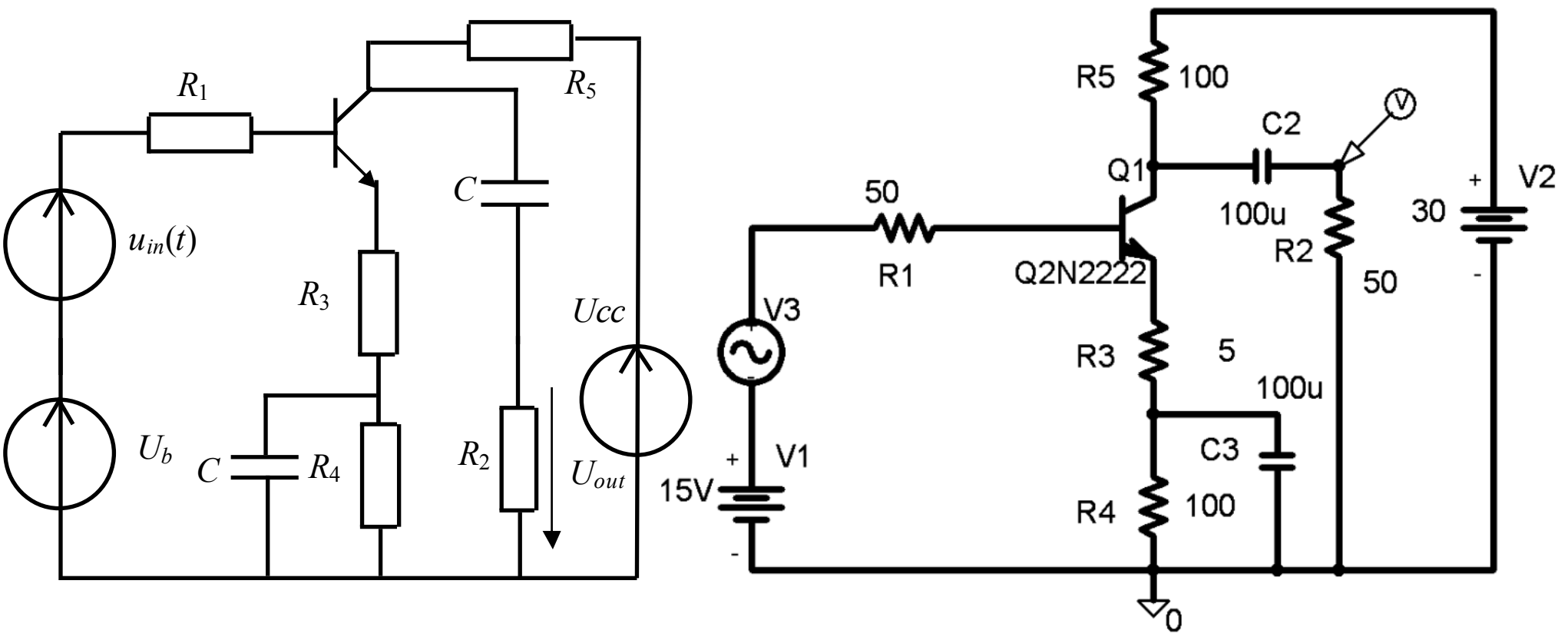

Figure 2. Scheme for virtual experiment 2

VE 2.1. In schematic module draw a scheme of NPN transistor with common emitter amplifier as shown on fig. 2.

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Use following parts: "**Q2N2222**" as a model of silicon NPN transistor 2N2222; "**r**" (five parts) as resistors; "**c**" (two parts) as capacitors; "**VDC**" (two parts) as models of DC sources; "**VSIN**" as a model of signal source; "**agnd**" as a ground (zero potential) sign.

Set the values of the resistances to following: signal source resistance (R_1) and load resistance (R_2) to 50 Ohm both; R_3 = 5 Ohm, R_4 = 100 Ohm, R_5 = 100 Ohm, capacitors to 100 μF.

Set power supply source (*Ucc*) to 30 V and displacement source (*Ub*) to 15 V. *Set* frequency of signal source to 1000 Hz, amplitude of voltage source to 0.1V, starting phase angle to 0.

Check **Transient** box in **Analysis-Setup** menu, enter the **Transient** dialogue box and set following parameters: **Print Step** = **Step ceiling** = 0.00001; **Final time** = 0.01.

VE 2.2. Simulate circuit and print (or copy-paste) the voltage curves. Explain the results.

VE 2.3. Change resistance R3 to 10 Ohm and repeat step **VE 2.2**.

VE 2.4. Change amplitude of signal source to 3 V and repeat step **VE 2.2**.

Virtual experiment 3.

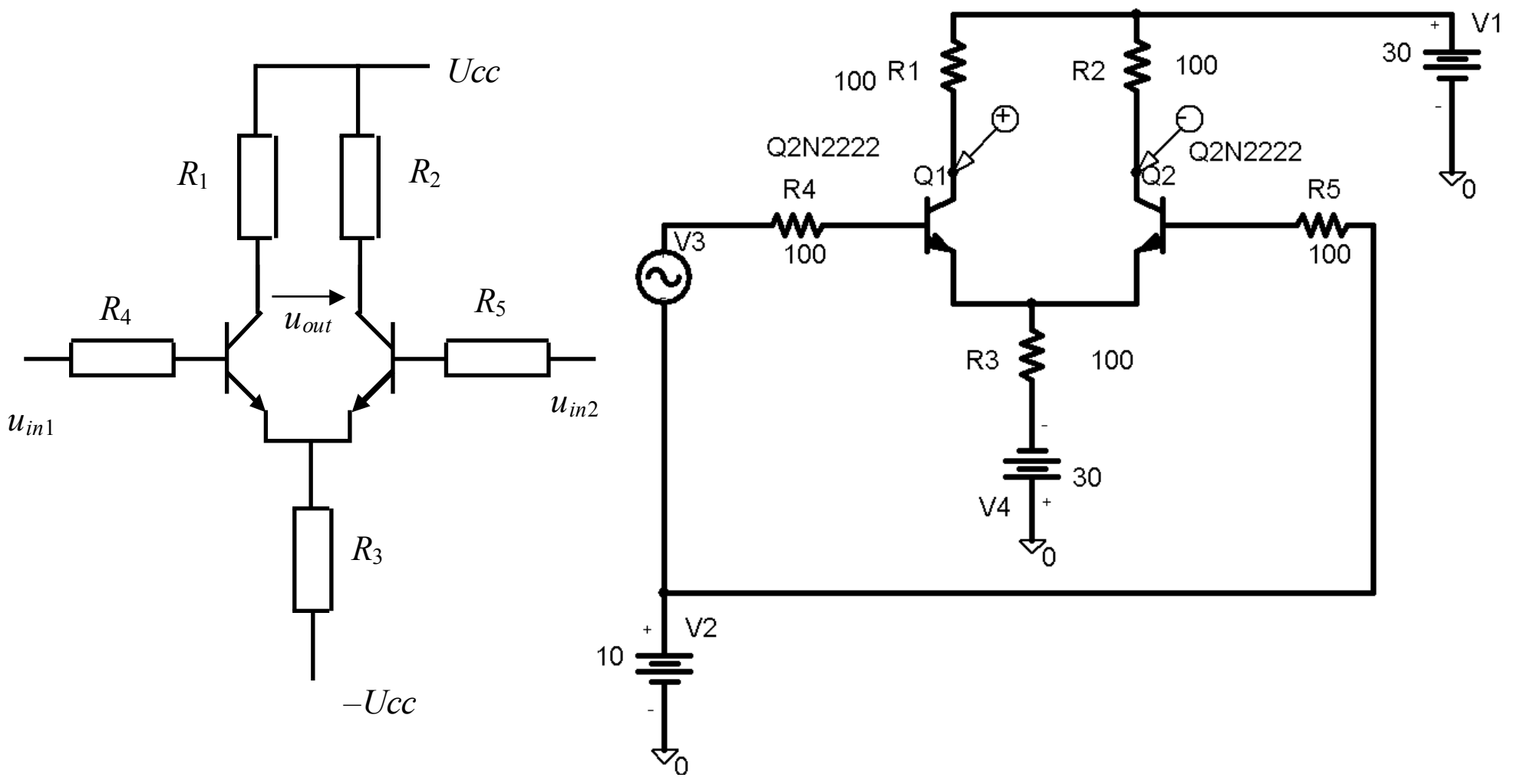

Figure 3. Scheme for virtual experiment 3

VE 3.1. In Schematic unit draw scheme of differential amplifier on the pair of NPN transistors as shown on fig. 3.

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Use following parts: "**Q2N2222**" (two parts) as models of silicon NPN transistors 2N2222; "**r**" (five parts) as resistors; "**VDC**" (three parts) as models of DC sources; "**VSIN**" as a model of signal source; "**agnd**" as a ground (zero potential) sign.

Set the values of the resistances to following: signal source resistances (R_1, R_2) to 100 Ohm; R_3 = 100 Ohm, R_4 = 100 Ohm, R_5 = 100 Ohm.

Set positive and negative power supply voltage sources to 30 V both and signal displacement source to 10 V. *Set* frequency of signal source to 1000 Hz, amplitude of signal source to 0.01V, starting phase angle to 0.

Check **Transient** box in **Analysis-Setup** menu, enter the **Transient** dialogue box and set following parameters: **Print Step** = **Step ceiling** = 0.00001; **Final time** = 0.01.

VE 3.2. Simulate circuit and print (or copy-paste) the voltage curves. Explain the results.

After work

Answer following questions:

a. What is the connection between base current collector, current and emitter current in different modes (cutoff, linear, saturation)?
b. Draw an Ebers-Moll equivalent scheme of NPN transistor.
c. What is the difference between PNP and NPN transistor linear amplifiers with common emitter?
d. What is the purpose of resistors R_3 and R_4 at fig. 2?
e. What is the purpose of capacitors C_1 and C_2?
f. What does limit the bandwidth of linear amplifier (fig. 2)?
g. What condition does limit the input voltage of linear amplifier (fig.2), differential amplifier (fig.3)?

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Laboratory work 3

Elementary circuits with MOS transistors

Content: metal-oxide-semiconductor field-effect transistors (MOS FETs), their characteristics, N-channel enhancement mode transistor with common (grounded) source, complimentary MOS (CMOS) pair.

Before work

a. Read the lectures on semiconductor physics, p-n junctions, MOS field-effect transistors, enhancement mode N-channel MOS transistor modes, linear amplifier on N-channel MOS transistor with common source, complimentary MOS (CMOS) pair.
b. Draw an approximate gate-source figure; show how steepness can be found.
c. Draw a scheme of linear amplifier on N-channel MOS transistor with common source. Write down formulas and equations for this circuit.
d. Draw a scheme CMOS pair. Draw a rough input-output figure in switcher mode.

Laboratory assignments

Virtual experiment 1

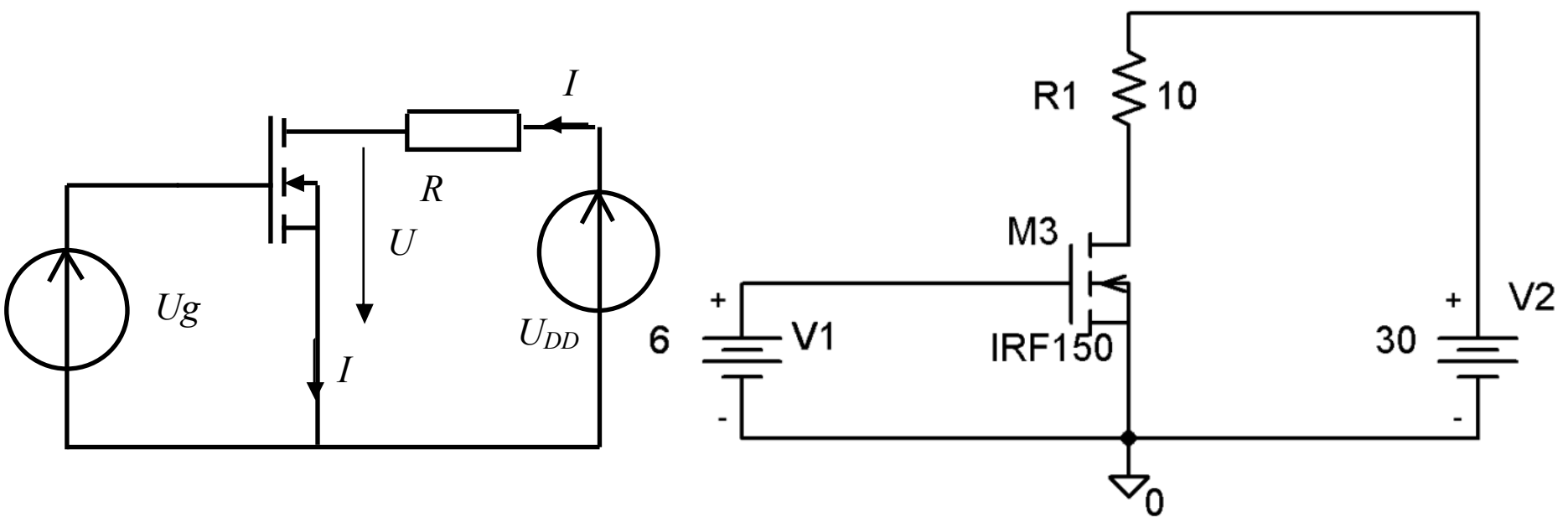

Figure 1. Scheme for virtual experiment 1

VE 1.1. In Design Center program (Schematic unit) draw a MOS N-channel transistor with common source scheme as shown on fig. 1.
Use following parts: "**IRF150**" as a model of power silicon MOSFET IRF150; "**r**" as a resistor; "**VDC**" (two parts) as models of the DC sources; "**agnd**" as a ground (zero potential) sign.

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Set resistance to 10 Ohm.
Set DC source (U_{DD}) to 30 V.

VE 1.2. Change gate displacement voltage value (voltage *Ug*), simulate circuit and measure drain–source voltage (*U*), drain current (*I*) in the circuit to complete following table:

Ug, V	0	2	2.75	2.9	3	3.1	3.3	3.5	3.75	4	5	6
U, V												
I, A												

VE 1.3. Draw a gate-drain characteristic of N-channel MOS transistor. Measure steepness (transconductance) in the middle of active region.

VE 1.4. Change U_{DD} to 15 V, repeat steps **VE 1.2** and **VE 1.3.**

Virtual experiment 2

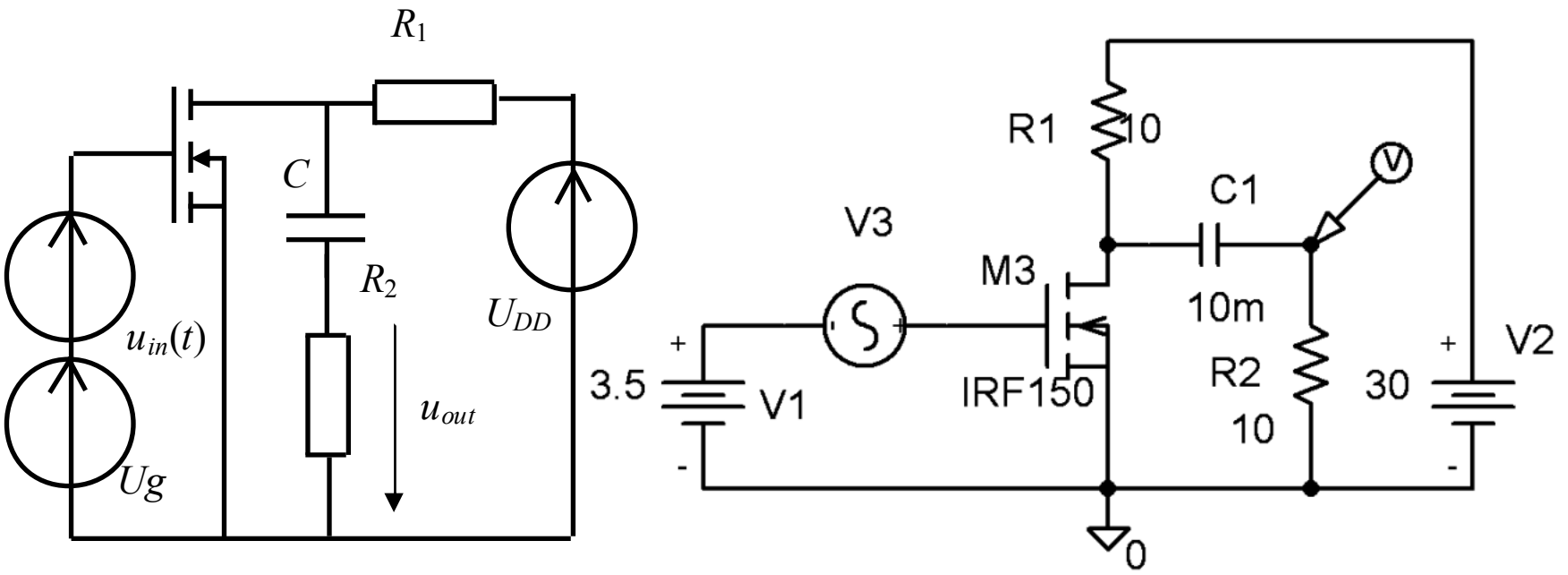

Figure 2. Scheme for virtual experiment 2

VE 2.1. Draw a scheme of linear amplifier on N-channel MOS transistor with common source as shown on fig. 2.
Use following parts: "**IRF150**" as a model of power silicon MOSFET IRF150; "**r**" (two parts) as resistors; "**c**" as a capacitor; "**VDC**" (two parts) as models of the DC sources; "**VSIN**" as a signal source; "**agnd**" as a ground (zero potential) sign.
Set the value of source resistance (R_1) to 10 Ohm; load resistance (R_2) to 100 Ohm; set capacity to 10 mF.
Set power supply (source) voltage source (U_{DD}) to 30 V; gate displacement voltage (*Ug*) to 3.5 V; frequency of signal source to 50 Hz, amplitude of signal source to 0.1 V, starting phase angle to 0.
Check **Transient** box in **Analysis-Setup** menu, enter the **Transient** dialogue box and set following parameters: **Print Step** = **Step ceiling** = 0.0001; **Final time** = 0.1.

VE 2.2. Simulate circuit and print (or copy-paste) the voltage curves. Explain the results.

VE 2.3. Change gate displacement voltage to 4 V and repeat step **VE 2.2.**

VE 2.4. Change resistance R_2 to 10 and repeat step **VE 2.2**.

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VE 2.5. Change amplitude of signal source to 2 V and repeat step **VE 2.2.**

Virtual experiment 3

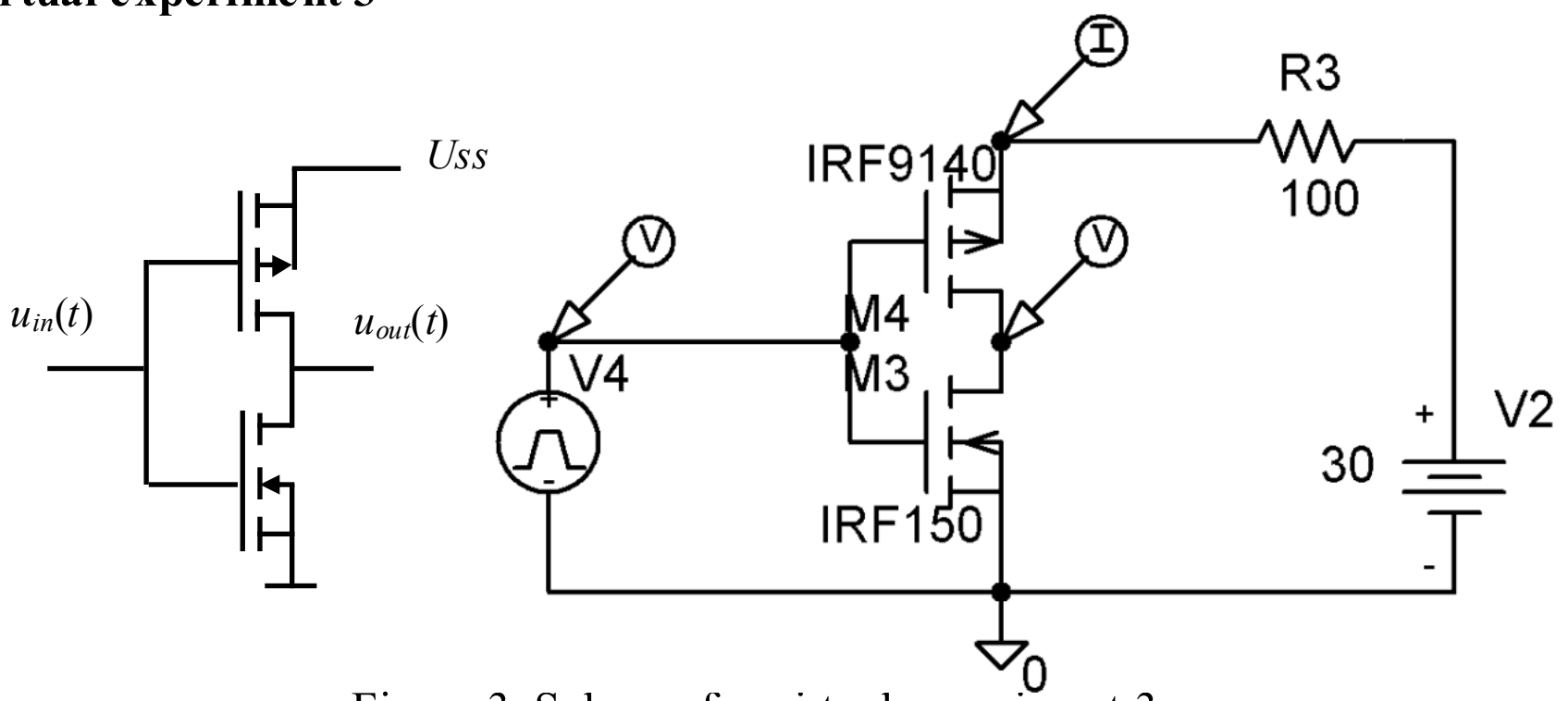

Figure 3. Scheme for virtual experiment 3

VE 3.1. In Schematic unit draw scheme of complimentary MOS transistor pair as shown on fig. 3.

Use following parts: "**IRF150**" as a model of power silicon N-channel MOSFET IRF150; "**IRF9140**" as a model of power silicon P-channel MOSFET IRF9140; "**r**" as a resistor; "**VDC**" as a model of DC source; "**VPULSE**" as a signal source; "**agnd**" as a ground (zero potential) sign; voltage and current probes as shown on fig. 3.

Set the value of the source resistance to 100 Ohm.

Set power supply source (*Uss*) to 30 V; set following parameters of pulse source: top voltage (**V1**) 25 V, floor voltage (**V2**) 2 V, delay time (**TD**) 1 ms, rise time (**TR**) and fall time (**TF**) 1 μs, pulse width (**PW**) 2 ms, period (**PER**) 4 ms.

Check **Transient** box in **Analysis-Setup** menu, enter the **Transient** dialogue box and set following parameters: **Print Step** = **Step ceiling** = 0.0001; **Final time** = 0.1.

VE 3.2. Simulate circuit and print (or copy-paste) the voltage curves. Explain results.

After work

Answer following questions:

a. What is a principle of field-effect transistor (FET) operating?
b. What is technology used for MOS transistor formation?
c. What is the difference between N and P-channel MOS transistors?
d. What is the purpose of resistors R_1 and R_2 at fig. 2?
e. What is the purpose of capacitor C?
f. What does limit the bandwidth of linear amplifier (fig. 2)?
g. What condition does limit the input voltage of linear amplifier (fig.2)?
h. What is the main advantage of complimentary MOS FET pair?

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Laboratory work 4

Logic gates and their applications

Content: integrated circuits (IC), logic gates, their static and dynamic characteristics; elementary circuits on logic gates – flip-flop, decoder.

Before work

a. Read the lectures on MOS transistors, CMOS FET pair, integrated circuits, logic gates, truth tables, memory cells, triggers, decoders, encoders, multiplexers, demultiplexers.
b. Draw scheme of the RS flip-flop on logic gates.
c. Draw a scheme of the 2-to-4 decoder.
d. Draw rough voltage diagrams on input/output of NAND and NOR logic gates.

Laboratory assignments

Virtual experiment 1

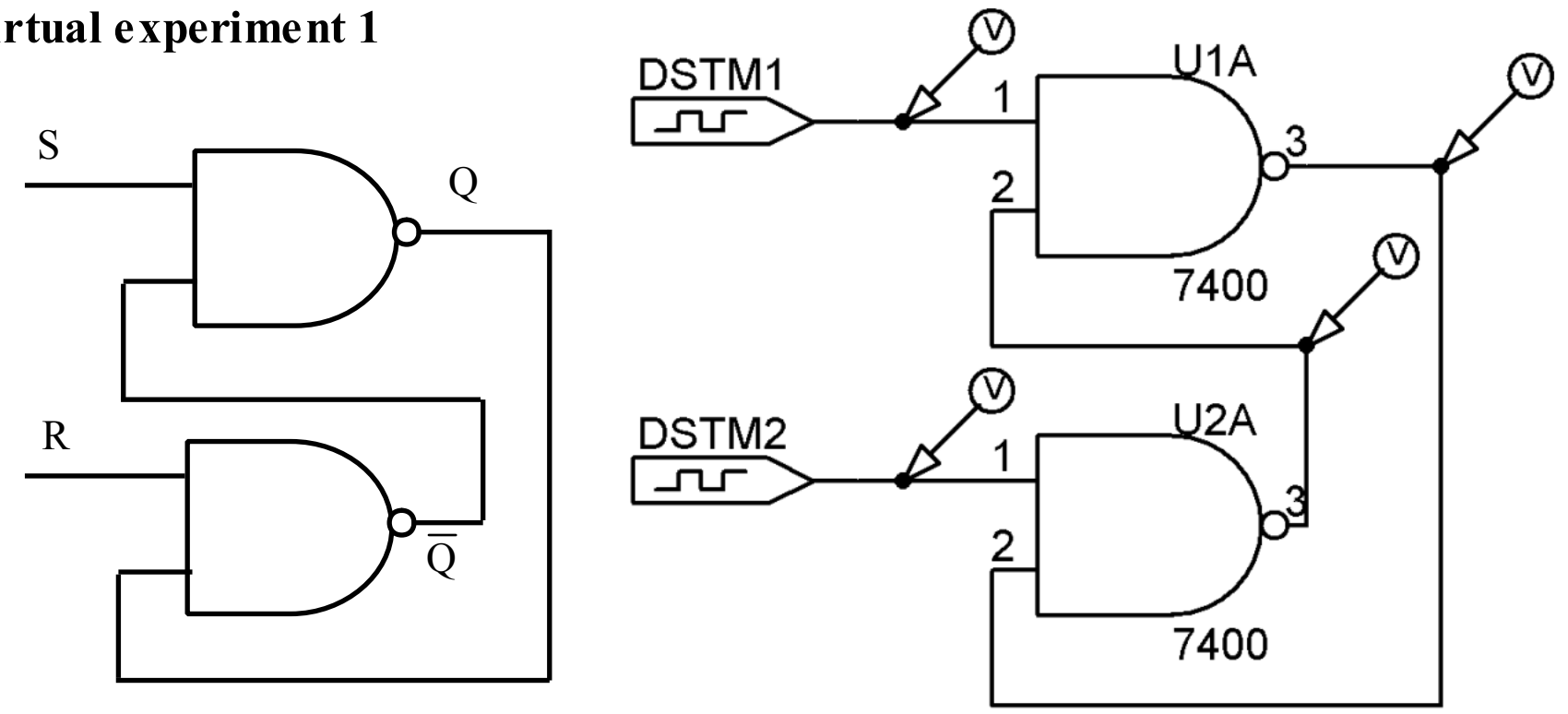

Figure 1. Scheme for virtual experiment 1

VE 1.1. In Schematic unit draw a scheme of RS flip-flop on NAND gates pair as shown on fig. 1.
Use following parts: "**7400**" (two parts) as models of NAND gate ICs 7400; "**STIM1**" (two parts) as models of digital input signals; voltage probes as shown on fig. 1.
Set time step of each **STIM1** block to 1 ms.
Set following commands for S input signal:
Command1 0ms 1
Command2 1ms 1
Command3 2ms 1

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Command4 3ms 0
Command5 4ms 1
Set following commands for R input signal:
Command1 0ms 1
Command2 1ms 0
Command3 2ms 1
Command4 3ms 1
Command5 4ms 1
Check **Transient** box in **Analysis-Setup** menu, enter the **Transient** dialogue box and set following parameters: **Print Step** = **Step ceiling** = 0.00001; **Final time** = 0.01.

VE 1.2. Simulate circuit and print (or copy-paste) timing diagrams. Explain the results.

Virtual experiment 2

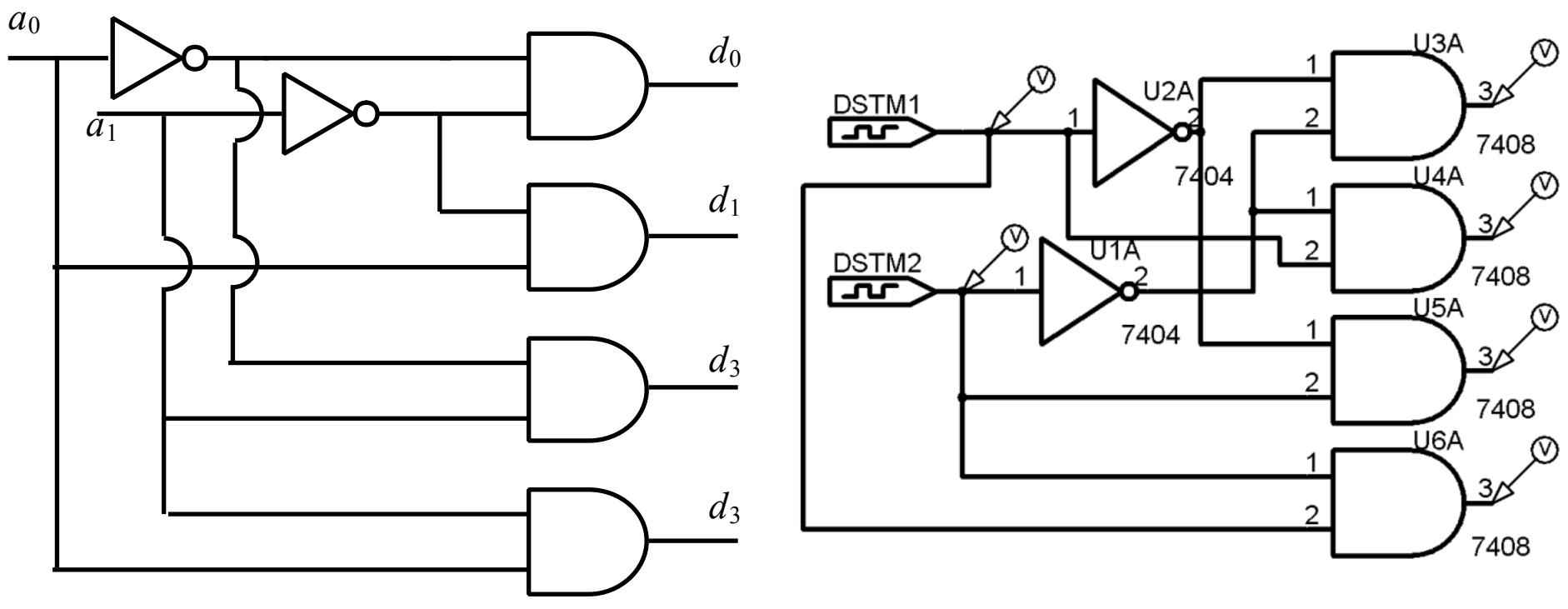

Figure 2. Scheme for virtual experiment 2

VE 2.1. In Schematic unit draw a scheme of 2-to-4 decoder as shown on fig. 2.
Use following parts: "**7408**" (four parts) as models of AND gate ICs 7408; "**7404**" (two parts) as models of NOT gate ICs 7404; "**STIM1**" (two parts) as models of digital input signals; voltage probes as shown on fig. 2.
Set time step of each **STIM1** block to 1 ms.
Set following commands for a_0 input signal:
Command1 0ms 0
Command2 1ms 1
Command3 2ms 0
Command4 3ms 1
S*et* following commands for a_1 input signal:
Command1 0ms 0
Command2 1ms 0
Command3 2ms 1
Command4 3ms 1

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Check **Transient** box in **Analysis-Setup** menu, enter the **Transient** dialogue box and set following parameters: **Print Step** = **Step ceiling** = 0.00001; **Final time** = 0.01.

VE 2.2. Simulate circuit and print (or copy-paste) timing diagrams. Explain the results.

After work

Answer following questions:

a. Fill truth-tables for AND, NAND, OR, NOR and XOR elements.
b. Which logic ICs families do you know?
c. What does limit operating frequency of logic gates ICs?
d. What are the purposes of logic gates at fig. 2?
e. Draw a scheme of multiplexer with four inputs.
f. Draw a scheme of demultiplexer with four outputs.
g. What shall we modify to increase number of input signals of the decoder?
h. What will happen when both R and S signals are enabled on RS flip-flop?
i. Draw a typical diagram of supply current for ICs on MOS FET technology.

Literature

1. **Sze S. M.,** Semiconductor Devices, Physics and Technology, *John Wiley*, 2nd edition, 2002
2. **Jaeger R. C**., Blalock T. N., Microelectronic Circuit Design, *McGraw-Hill*, 3rd edition, 2008

Contents

Учебное издание
Вишняков Сергей Викторович, **Вишнякова** Юлия Николаевна
МОДЕЛИРОВАНИЕ ЭЛЕКТРОННЫХ ЦЕПЕЙ. ЛАБОРАТОРНЫЕ РАБОТЫ 1-4
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